4.9152Gbps Sub Channel BIDI SFP Transceiver

Features

- Up to 4.9152Gbps data rate
- Standard Small Form Pluggable package with receptacle LC/UPC connector
- Compliant with SFP MSA
- SFF-8472 compliant digital diagnostic monitoring function implemented
- Internally calibrated mode
- Cooled DFB laser transmitters
- High sensitive PIN photodiode
- Single +3.3V power supply
- Operating case temperature; -40℃ to +85℃
- Differential CML inputs and outputs
- Internally AC-Coupled electrical interface
- RoHS compliant

Description

IBP-C5SxxyB-I12R Sub Channel SFP transceivers are designed to meet serial optical data communications specification. The transceivers are manufactured in hot pluggable capability package with receptacle LC connector interface and made of metallized housing to obtain excellent EMI shielding.

The transmitter consists of DFB laser in an optical subassembly (OSA).

The OSA is driven by a custom IC which converts differential CML logic signals into a laser diode drive current. The receiver includes a planar InGaAs PIN-PD mounted with a transimpedance preamplifier IC in an OSA. The OSA is mated to a custom limiting-amplifier which provides post-amplification and signal detect function (Logic 0 indicates normal operation).

The transceivers are designed to used in a single power supply (+3.3V) and an operating temperature range of -40℃ to +85℃

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Applications

- Digital Wireless Repeaters
- Digital Wireless BTS Interconnects: CPRI 4.9152Gbps Standards
- Metro Access Rings
- High-speed data links.

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Unit
Storage Temperature	T_{ST}	-40		+85	℃
Power Supply Voltage	V_{CC}	0.5		4.0	V
Operating Humidity	H_{OP}			85	% RH

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Operating Case Temperature	T_C	-40(T_A)		+85(T_C)	℃
Supply Voltage	V_{CC}	3.15	3.3	3.45	V
Power Supply Current	$I_{cc(Tx+Rx)}$			550	mA

CWDM Wavelength

Parameter	Symbol	Low	Symbol	High	Unit
O-band Original	λ_L	1266	λ_H	1275.5	nm
	λ_L	1286	λ_H	1295.5	nm
	λ_L	1306	λ_H	1315.5	nm
	λ_L	1326	λ_H	1335.5	nm
	λ_L	1346	λ_H	1355.5	nm
E-band Extended	λ_L	1366	λ_H	1375.5	nm
	λ_L	1386	λ_H	1395.5	nm
	λ_L	1406	λ_H	1415.5	nm
	λ_L	1426	λ_H	1435.5	nm
	λ_L	1446	λ_H	1455.5	nm
S-band Short Wavelength	λ_L	1466	λ_H	1475.5	nm
	λ_L	1486	λ_H	1495.5	nm
	λ_L	1506	λ_H	1515.5	nm
	λ_L	1526	λ_H	1535.5	nm
C-band Conventional	λ_L	1546	λ_H	1555.5	nm
L-band Long Wavelength	λ_L	1566	λ_H	1575.5	nm
	λ_L	1586	λ_H	1595.5	nm
	λ_L	1606	λ_H	1615.5	nm

Transmitter Characteristics

Parameter		Symbol	Min	Typ	Max	Unit
Bit rate		B		4.9152		Gbps
Wavelength	Low	λ	λ_L - 3.5	λ_L	λ_L + 3.5	nm
	High		λ_H - 2.5	λ_H	λ_H + 2	
Output Spectral Width (-20dB)		Δλ			1	nm
Average Launch Power		P_o	-3		+2	dBm
Extinction ratio		dB	4.5			dB
Side Mode Suppression Ratio		SMSR	30			dB
Differential data input swing		$V_{IN, p-p}$	500		2000	mV
TX_Disable Input High Voltage		V_{IH}	2		Host Vcc	V
TX_Disable Input Low Voltage		V_{IL}			0.8	V
TX_Fault Output High Voltage		V_{OH}	2		Host Vcc	V
TX_Fault Output Low Voltage		V_{OL}	0		0.8	V

Receiver Characteristics

Parameter		Symbol	Min	Typ	Max	Unit
Bit rate		B		4.9152		Gbps
Wavelength	Low	λ	λ_H - 2.5	λ_H	λ_H + 2	nm
	High		λ_L - 3.5	λ_L	λ_L + 3.5	
Differential data output swing		$V_{OUT, p-p}$	400	800	1000	mV
RX_LOS Output Voltage-high		V_{OH}	2		Host Vcc	V
RX_LOS Output Voltage-Low		V_{OL}	0		0.4	V
Average Rx Sensitivity (Note 1)		P_{min}			-15	dBm
Maximum Input Power		P_{max}	+1			dBm
LOS De-Assert		LOS_D			-17	dBm
LOS Assert		LOS_A	-35			dBm
LOS Hysteresis		LOS_{HYS}	0.5			dB

Note 1) Minimum sensitivity and saturation level at 2.5Gbps, BER $1x10^{-12}$ for a 2^{23}-1 PRBS.

Block Diagram

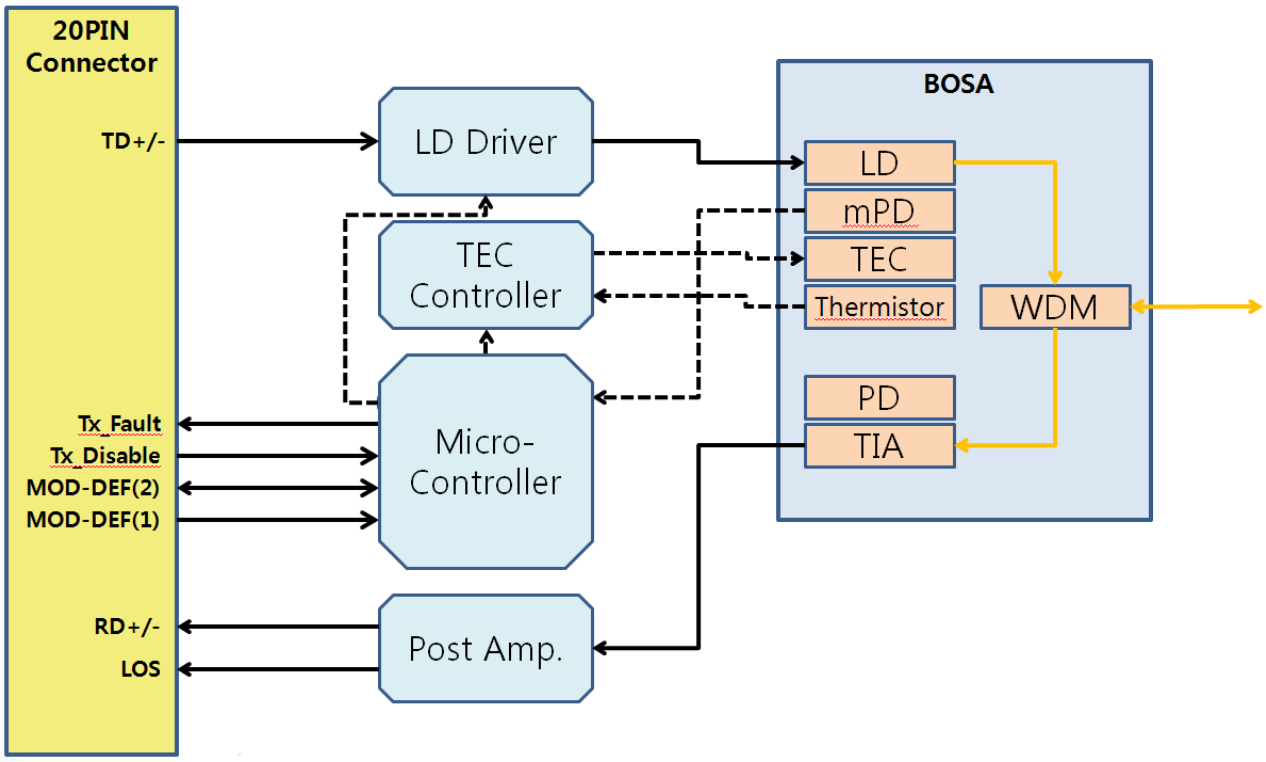

Fig. 1 Block Diagram

PIN description

These devices can be installed in or removed from any MSA-compliant Pluggable Small Form Factor port regardless of whether the host equipment is operating or not. These devices are simply inserted, electrical-interface first, under finger-pressure. Controlled hot-plugging is ensured by 3-stage pin sequencing at the electrical interface. See the Fig. 2 as these devices are inserted, first contact is made by the housing ground shield, discharging any potentially component-damaging static electricity. Ground pins engage next and are followed by TX and RX power supplies. Finally, signal pins are connected.

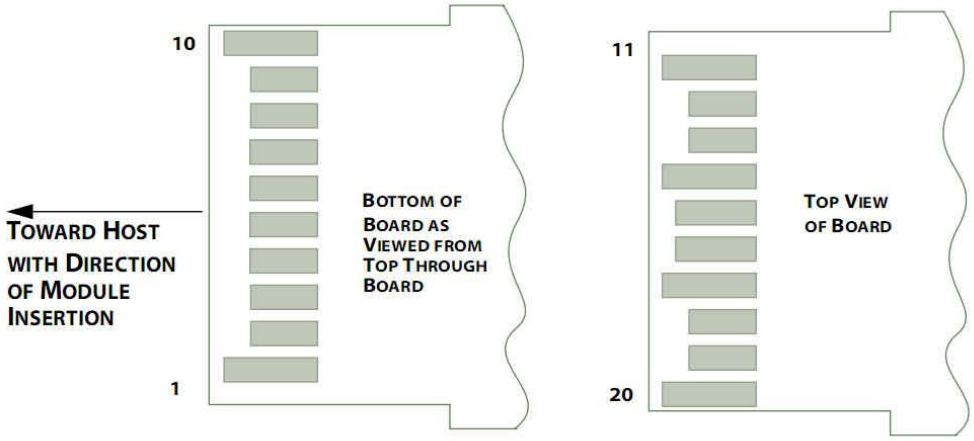

Fig. 2 SFP Transceiver Electrical Pad Layout

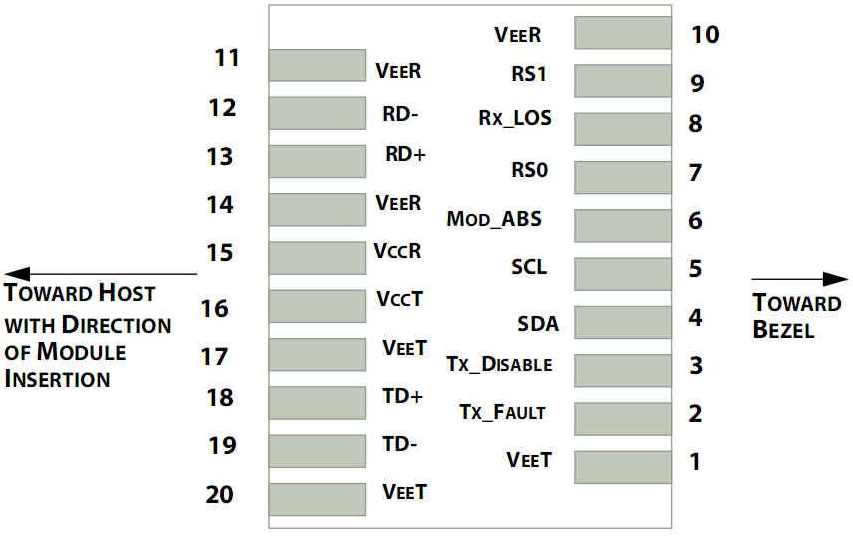

Fig. 3 Host PCB SFP Pin-out

PIN assignment

Pin	Name	In/Out	Logic	Description	Note
1	VeeT			Module Transmitter Ground	
2	TX_Fault		LVTTL	Module Transmitter Fault	2
3	TX_Dis	I	LVTTL	Transmitter Disable; Turns off transmitter laser output	3
4	SDA	I/O	LVTTL	2-Wire Serial Interface Data Line	
5	SCL	I/O	LVTTL	2-Wire Serial Interface Clock	
6	Mod_ABS			Module Absent, connected to VeeT or VeeR in the module	2
7	Rate Select		LVTTL	No connection required	
8	RX_LOS	O	LVTTL	Receiver Loss Of Signal Indication (In FC designated as RX_LOS and in Ethernet designated as Signal Detect)	2
9	VeeR			Module Receiver Ground	
10	VeeR			Module Receiver Ground	1
11	VeeR			Module Receiver Ground	1
12	RD-	O	CML	Receiver Inverted Data Output	
13	RD+	O	CML	Receiver Non-Inverted Data Output	
14	VeeR			Module Receiver Ground	1
15	VccR			Module Receiver 3.3 V Supply	
16	VccT			Module Transmitter 3.3 V Supply	
17	VeeT			Module Transmitter Ground	1
18	TD+	I	CML	Transmitter Non-Inverted Data Input	
19	TD-	I	CML	Transmitter Inverted Data Input	
20	VeeT			Module Transmitter Ground	1

Note

1: Module ground pins are isolated from the module case and chassis ground within the module.

2: Shall be pulled up with 4.7k to 10k ohm to a voltage between 3.15V and 3.45V on the host board.

3: Shall be pulled up with 4.7k to 10k ohm to VccT in the module.

Timing Characteristics

Parameter	Symbol	Min	Max	Unit	Condition
TX_DISABLE Assert Time	t_off		10	us	Time from rising edge of TX_DISABLE to when the optical output falls below 10% of nominal
TX_DISABLE Negate Time	t_on		1	ms	Time from falling edge of TX_DISABLE to when the modulated optical output rises above 90% of nominal
Time to Initialize, Including Reset of TX_FAULT	t_init		300	ms	From power on or negation of TX_FAULT using TX_DISABLE
TX_FAULT Assert Time	T_fault		100	us	Time from fault to TX_FAULT on
TX_DISABLE to Reset	T_reset	10		us	Time TX_DISABLE must be held high to reset TX_FAULT
RX_LOS Assert Time	t_loss_on		100	us	Time from LOS state to RX_LOS Assert
RX_LOS Negate Time	t_loss_off		100	us	Time from non-LOS state to RX_LOS deassert

Two-wire Interface Protocol

The Intec E&C SFP transceiver supports a two-wire management interface as specified in the SFP MSA. Two-wire bus timing is shown in Fig. 4. SFP 2-wire timing specifications are given in Table 1.

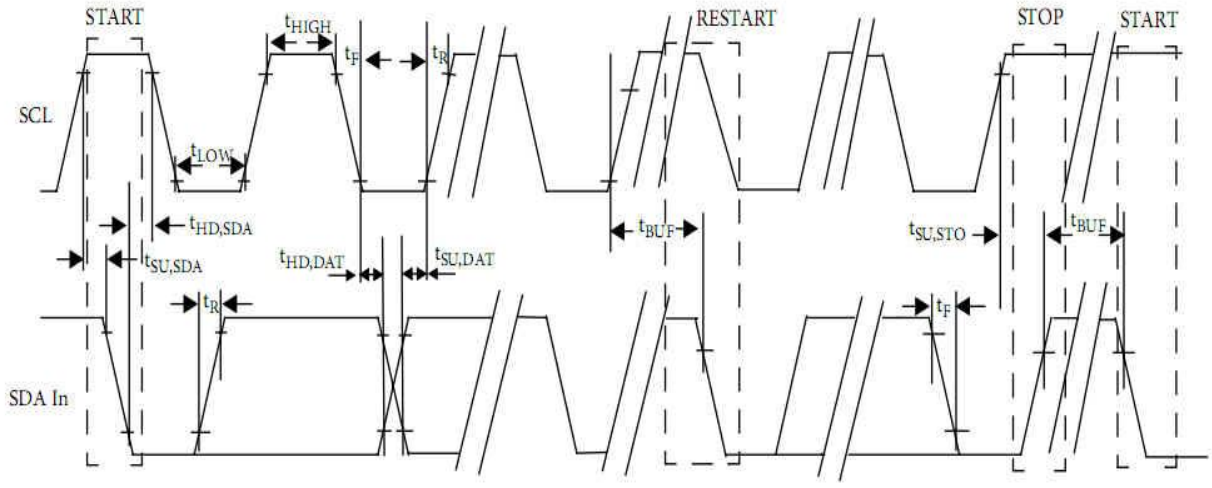

Fig. 4 2-wire timing diagram

Table 1.

Parameter	Symbol	Min	Max	Unit	Condition
Clock Frequency	f_{SCL}	0	400	kHz	Module shall operate with up to 100kHz without requiring clock stretching. The module may clock sretch with greater than 100kHz and up to 400kHz
Clock Pulse Width Low	t_{LOW}	1.3		μs	
Clock Pulse Width High	t_{HIGH}	0.6		μs	
Time bus free before new transmission can start	t_{BUF}	20		μs	Between STOP and START and ACK and ReSTART
START Hold Time	$t_{HD,STA}$	0.6		μs	
START Set-up Time	$t_{SU,STA}$	0.6		μs	
DATA In Hold Time	$t_{HD,DAT}$	0		μs	
DATA In Set-up Time	$t_{SU,DAT}$	0.1		μs	
Input Rise Time (100KHz)	$t_{R,100}$		1000	ns	From ($V_{IL,MAX}$-0.15) to ($V_{IH,MIN}$+0.15)
Input Rise Time (400KHz)	$t_{R,400}$		300	ns	From ($V_{IL,MAX}$-0.15) to ($V_{IH,MIN}$+0.15)
Input Fall Time (100KHz)	$t_{F,100}$		300	ns	From ($V_{IH,MIN}$+0.15) to ($V_{IL,MAX}$-0.15)
Input Fall Time (400KHz)	$t_{F,400}$		300	ns	From ($V_{IH,MIN}$+0.15) to ($V_{IL,MAX}$-0.15)
STOP Set-up Time	$t_{SU,STO}$	0.6		μs	

SFP Host Board Mechanical Layout [unit: mm]

A typical host board mechanical layout for attaching the SFP connector and cage system is shown in Fig. 5 and Fig. 6.

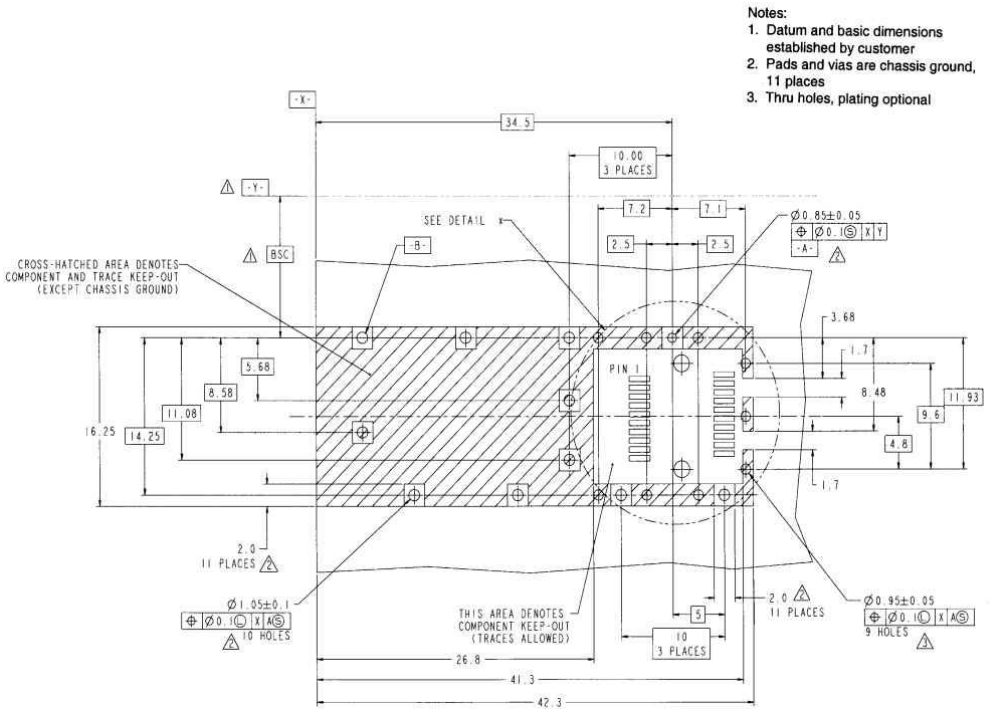

Fig. 5 Host board mechanical layout (mm)

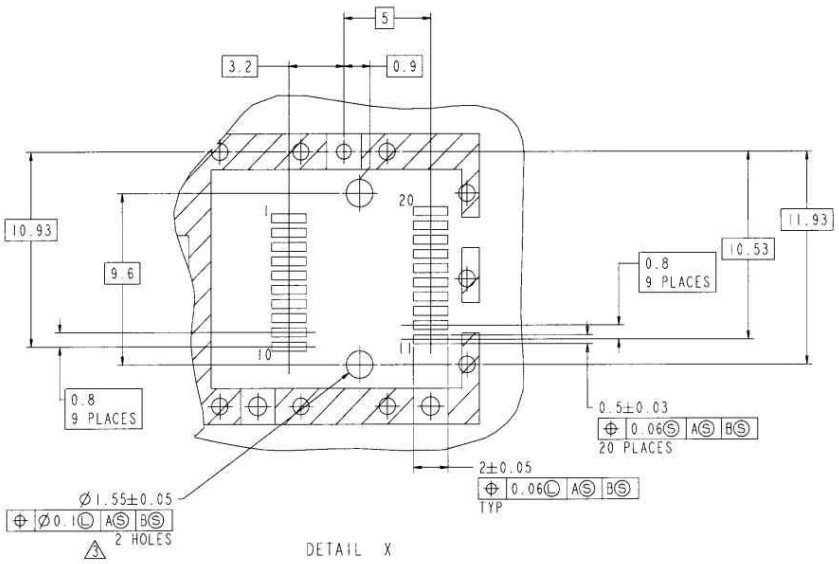

Fig. 6 Detailed host board mechanical layout (mm)

Host Board Power Supply filtering

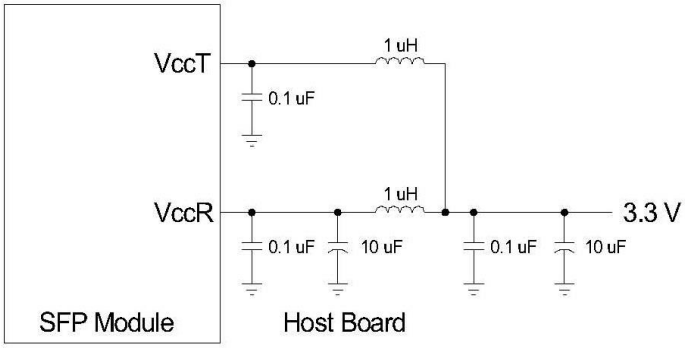

Fig. 7 Host board power supply filtering

Recommended Circuit Schematic

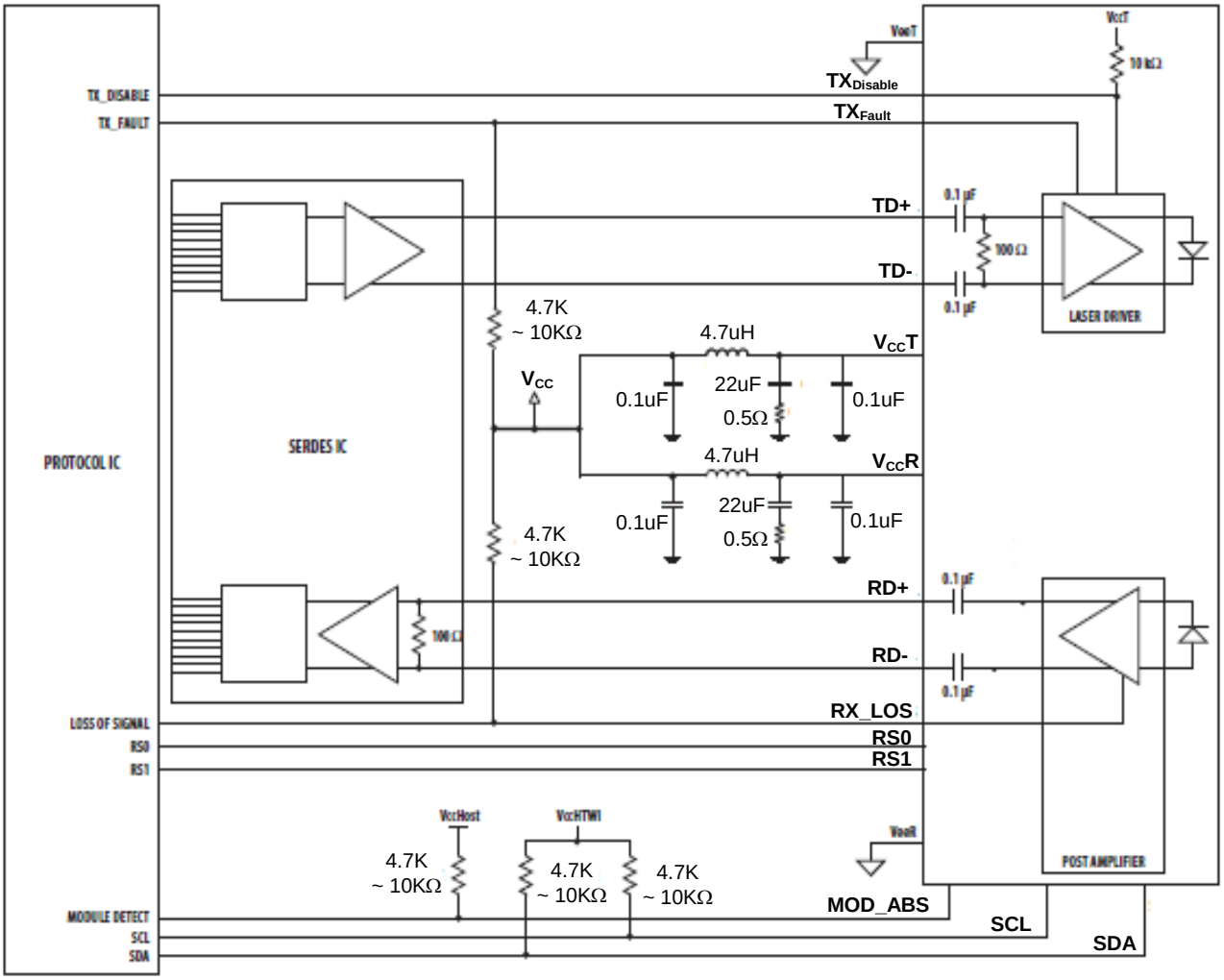

Fig. 8 SFP Host board Schematic Application

Digital Diagnostic Functions

The IBP-C5SxxyB-I12R Sub Channel SFP transceivers support the 2-wire serial communication protocol (I^2C) as defined in the SFP MSA. Through this serial communication, these transceivers provide access to identification information that describes their capabilities, standard interfaces, manufacturer, and other information. In addition, these SFP transceivers provide enhanced digital diagnostic monitoring interface, which allows real-time access to device operating conditions such as internal temperature, laser bias current, transmitted optical power, received optical power and supply voltage. It also defines a sophisticated system of alarm and warning flags.

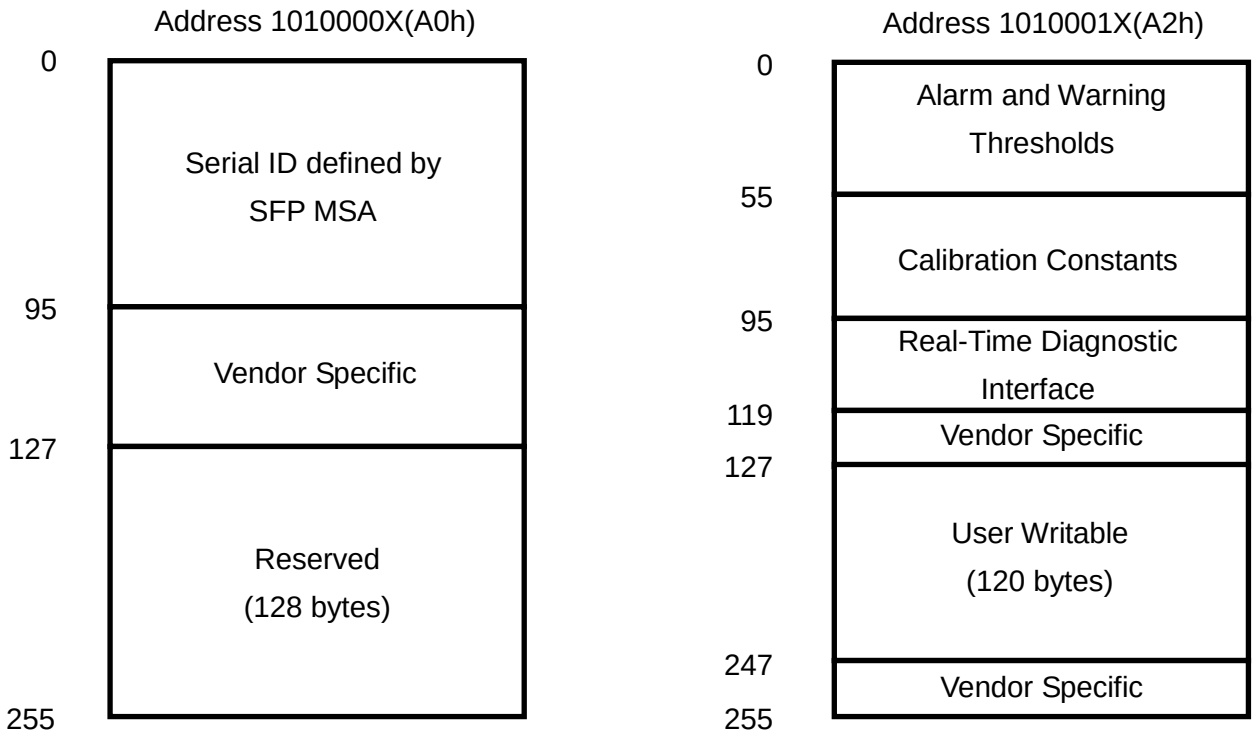

Fig. 9 Two-wire serial digital memory map

Ordering Information

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No.	ITEM	Code	Description
①	Company	I	INTEC E&C
②	Form Factor	BP	BIDI CWDM SFP
③	Data-rate	C5	4.9152Gbps
④	CWDM wavelength select	Sxx	Sub Channel, 27(1270nm)~61(1610nm)
⑤	Tx wavelength select	y	L(Low), H(High)
⑥	Optical interface	B	LC-UPC receptacle
⑦	Temperature range	I	-40℃ ~ 85℃
⑧	Link budget	12	12dB
⑨	RoHS	R	RoHS compliant

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