Preliminary RoHS Compliant

100G LC Duplex QSFP28 LR4 Transceiver

[IQ2-CELRLWB-S04I]

Key Features

- QSFP28 Transceivers
- Compliant with MSA QSFP28 specification
- Single +3.3V Power Supply
- Duplex LC Connector
- Supports 100G Ethernet and OTU4

◆ Features

- **Integrated LAN-WDM TOSA/ROSA**
- **LC Duplex optical receptacle**
- **Compliant CAUI-4**
- **Operating case temperature range from 0℃ to 70℃**
- **Low power consumption: Max. 3.5W**
- **Hot-pluggable to 38-pin electrical interface**
- **2-wire management interface**
- **Class 1 Laser safety**
- **RoHS 6/6 compliant**

◆ Applications

- **Local area networks**
- **Wide area networks**
- **100G Ethernet switches and routers**
- **Storage area networks**

1. Functional Description

The transceiver is the QSFP28 optical transceiver module which is a hot pluggable form factor designed for high speed optical networking application. The transceiver is designed for 100Gigabit Ethernet application and provides 100GBASE-LR4 compliant optical interface, CAUI-4 electrical interface and 2-wire management interface. The transceiver converts 4-lane 25Gb/s electrical data streams to 4-lane LAN-WDM 25Gb/s optical output signal and 4-lane LAN-WDM 25Gb/s optical input signal to 4-lane 25Gb/s electrical data streams.

The high performance LAN-WDM DFB-LD transmitter and high sensitivity PIN receiver provide superior performance for 100Gigabit Ethernet applications up to 10km links and compliant optical interface with IEEE802.3ba Clause 100GBASE-LR4 requirements.

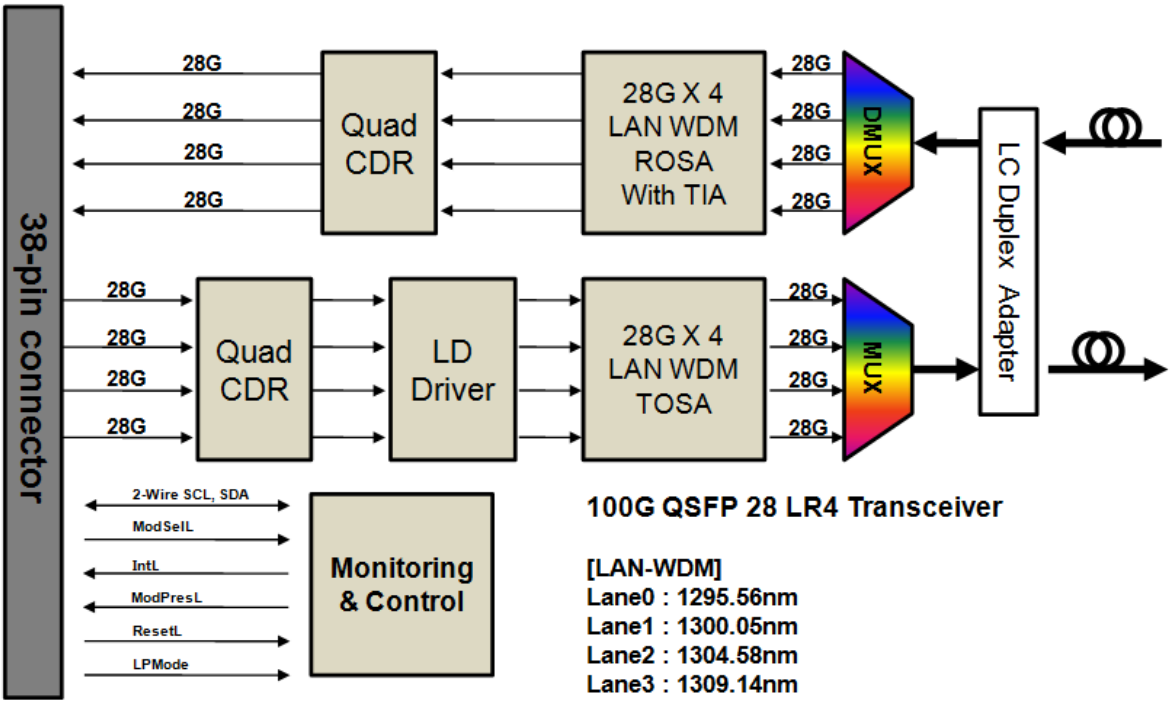

Figure 1. Transceiver block diagram

1.1 Transmitter

The transmitter inputs are connected to four laser driver circuits, each of which transforms the small swing digital voltage to an output modulation that drives a DFB laser. The four laser optical output signals are combined using a LAN-WDM optical multiplexer and coupled into a single mode fiber through an industry standard LC optical connector. Control of the transmitted power and modulation swing over temperature and voltage variations is provided.

1.2 Receiver

The receiver converts the incoming four lanes of NRZ optical data into four lanes of CAUI-4 electrical data. The four incoming wavelengths are separated by a LAN-WDM optical demultiplexer with each output coupled to a PIN photodetector. The electrical currents from each PIN photodetector are converted to a voltage in a high-gain transimpedance amplifier.

1.3 Low Speed Description

1.3.1 Low Speed Pin Descriptions

The transceiver has several low-speed interface connectors including a 2-wire serial interface (SCL and SDA). These connections include: Module Select(ModSelL), Reset(ResetL), Low Power Mode(LPMode), Module Present(ModPrsL) and Interrupt(IntL).

[ModSelL]

The ModSelL is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple modules on a single 2-wire interface bus. When the ModSelL is "High", the module shall not respond to or acknowledge any 2-wire interface communication from the host. ModSelL signal input node shall be biased to the "High" state in the module.

In order to avoid conflicts, the host system shall not attempt 2-wire interface communications within the ModSelL de-assert time after any modules are deselected. Similarly, the host shall wait at least for the period of the ModSelL assert time before communicating with the newly selected module. The assertion and de-asserting periods of different modules may overlap as long as the above timing requirements are met**.**

[ResetL]

The ResetL pin shall be pulled to Vcc in the module. A low level on the ResetL pin for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time (t_init) starts on the rising edge after the low level on the ResetL pin is released. During the execution of a reset (t_init) the host shall disregard all status bits until

the module indicates a completion of the reset interrupt. The module indicates this by asserting "low" an IntL signal with the Data_Not_Ready bit negated. Note that on power up (including hot insertion) the module should post this completion of reset interrupt without requiring a reset.

[LPMode]

The LPMode pin shall be pulled up to Vcc in the module. The pin is a hardware control used to put

modules into a low power mode when high. By using the LPMode pin and a combination of the Power_override, Power_set and High_Power_Class_Enable software control bits (Address A0h, byte 93 bits 0,1,2).

[ModPrsL]

ModPrsL is pulled up to Vcc_Host on the host board and grounded in the module. The ModPrsL is asserted "Low" when inserted and deasserted "High" when the module is physically absent from the host connector.

[IntL]

IntL is an output pin. When IntL is "Low", it indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL pin is an open collector output and shall be pulled to host supply voltage on the host board. The INTL pin is deasserted "High" after completion of reset, when byte 2 bit 0 (Data Not Ready) is read with a value of '0' and the flag field is read.

1.3.1 Low Speed Pin Electrical Specifications

[Low Speed Signaling]

Low speed signaling other than SCL and SDA is based on Low Voltage TTL (LVTTL) operating at Vcc. Vcc refers to the generic supply voltages of VccTx, VccRx, Vcc_host or Vcc1.

Hosts shall use a pull-up resistor connected to Vcc_host on each of the 2-wire interface SCL (clock), SDA (data), and all low speed status outputs.

The SCL and SDA is a hot plug interface that may support a bus topology. During module insertion or removal, the module may implement a pre-charge circuit which prevents corrupting data transfers from other modules that are already using the bus.

Table 1. Low Speed Pin Electrical Specifications

Parameter	Symbol	Min	Max	Unit	Condition
SCL and SDA	VOL	0		V	IOL(max)=3.0mA
	VOH	Vcc-0.5	Vcc+0.3	V	
SCL and SDA	VIL	-0.3	Vcc*0.3	V	
	VIH	Vcc*0.7	Vcc+0.5	V	
Capacitance for SCL and SDA I/O Pin	Ci		14	pF	
Total bus capacitive load for SCL and SDA	Cb		100	pF	3.0KΩ Pull-up resistor, Max
			200	pF	1.6KΩ Pull-up resistor, Max
LPMode, Reset and ModSelL	VIL	-0.3	0.8	V	|Iin|<=125uA for 0V<Vin, Vcc
	VIH	2	Vcc+0.3	V	

ModPrsL and IntL	VOL	0	0.4	V	IOL=2.0mA
	VOH	Vcc-0.5	Vcc+0.3	V	

[2-wire Timing Daigram]

The transceiver 2-wire bus timing is shown in Fig 2. and the detail of clock stretching is shown in Figure 3. The transceiver 2-wire timing specifications are given in Table 2.

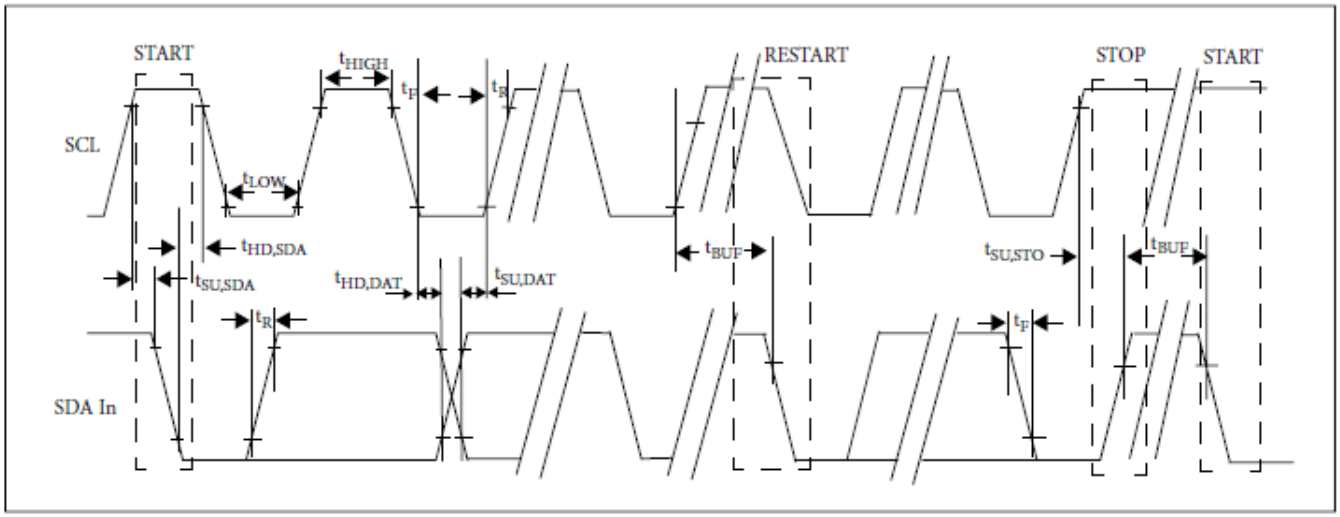

Fig 2. Two wire interface timing diagram

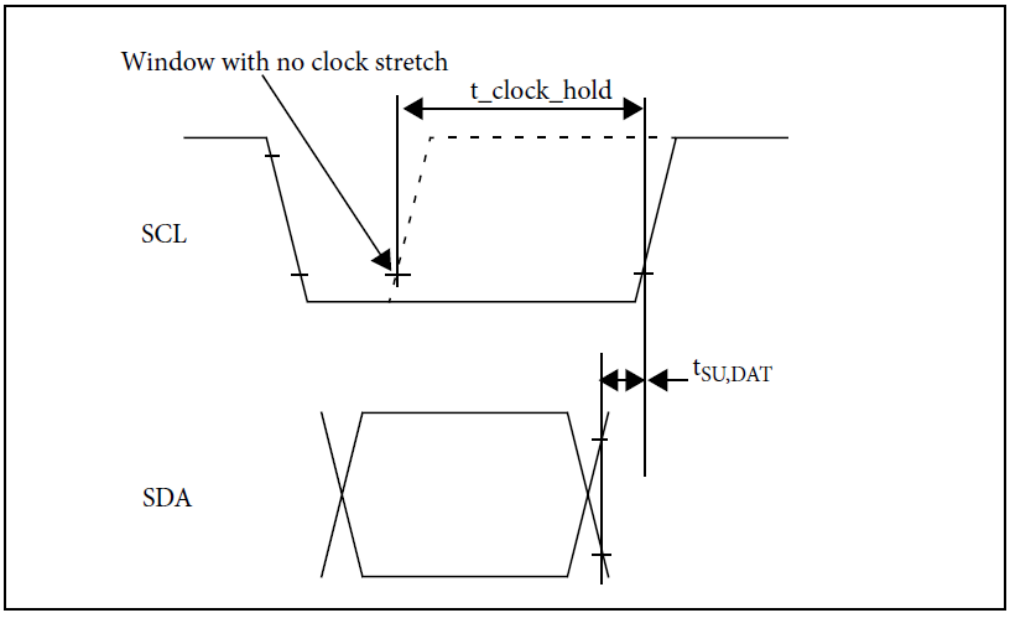

Fig 3. Detail of Clock Stretching

Table 2. MANAGEMENT INTERFACE TIMING PARAMETERS

Parameter	Symbol	Min	Max	Unit	Conditions
Clock Frequency	fSCL	0	400	kHz	
Clock Pulse Width Low	tLOW	1.3		us	
Clock Pulse Width High	tHIGH	0.6		us	
Time bus free before new transmission can start	tTUF	20		us	Between STOP and START and between ACK and ReStart
START Hold Time	tHD.STA	0.6		us	
START Set-up Time	tSU.STA	0.6			
Data In Hold Time	tHD.DAT	0			
Data in Set-up Time	tSU.DAT	0.1			
Input Rise Time (400 kHz)	tR.400		300	ns	From (VIL,MAX-0.15) to (VIH, MIN +0.15)
Input Fall Time (400 kHz)	tF.400		300	ns	From (VIH,MIN + 0.15) to (VIL,MAX - 0.15)
STOP Set-up Time	tSU.STO	0.6		us	
Serial Interface Clock Holdoff (ClockStretching)	T_cLock_hold		500	us	Maximum time the slave may hold the SCL line low before continuing with a read or write operation

2. Application

Recommended MSA connections to the transceiver are shown in Figure 4 below.
Power supply filtering is recommended for the transceiver.

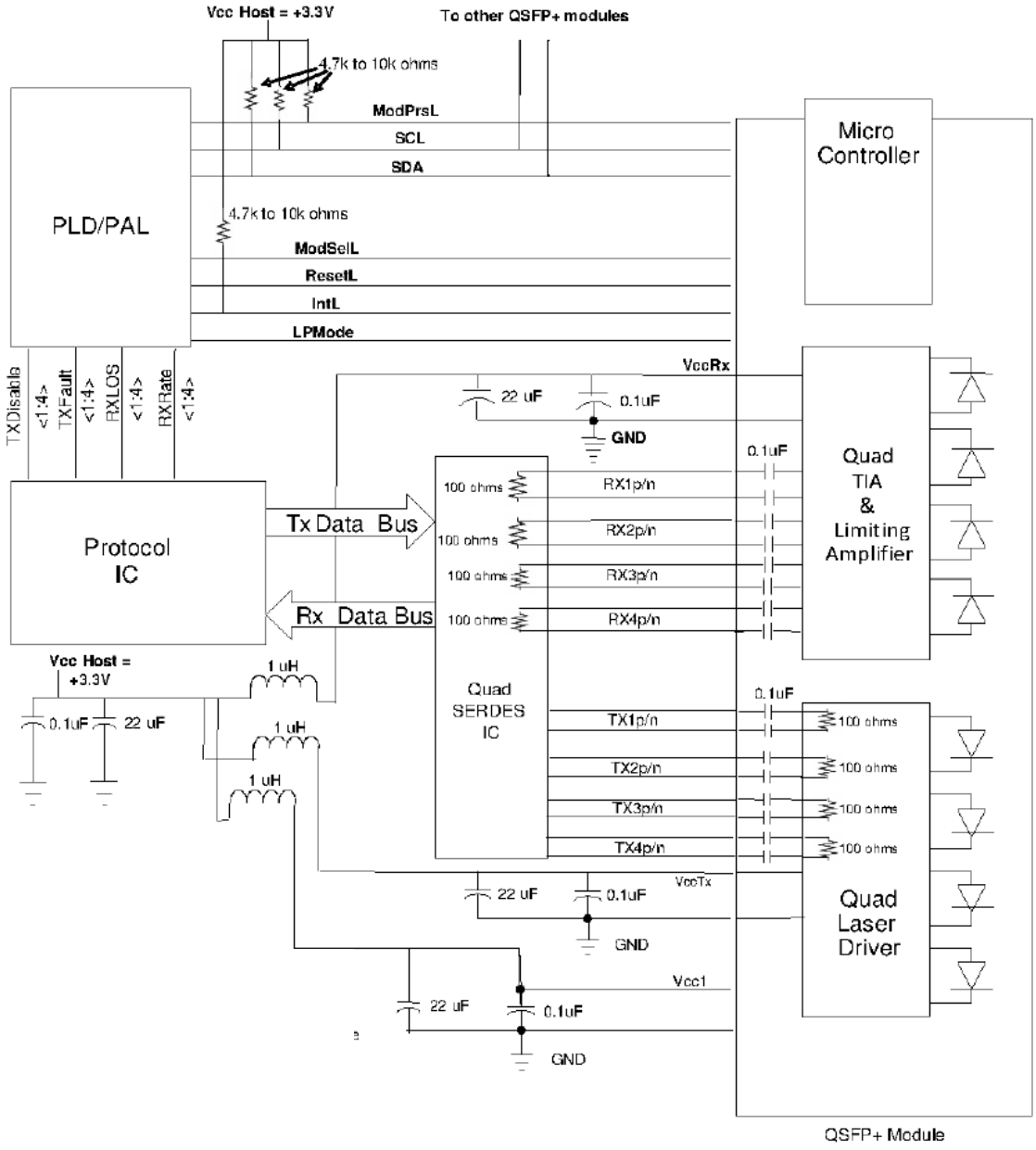

Fig 4. Host Board Schematic

Note1 : Decoupling capacitor values are informative and vary depending on applications.

Note2 : Vcc1 connection may be connected to Vcc Tx or Vcc Rx provided the applicable derating of the maximum current limit is used.

3. PIN description

Figure 5 shows the signal symbols and contact numbering for the module edge connector. The diagram shows the module PCB edge as a top and bottom view. There are 38 contacts intended for high speed signals, low speed signals, power and ground connections.

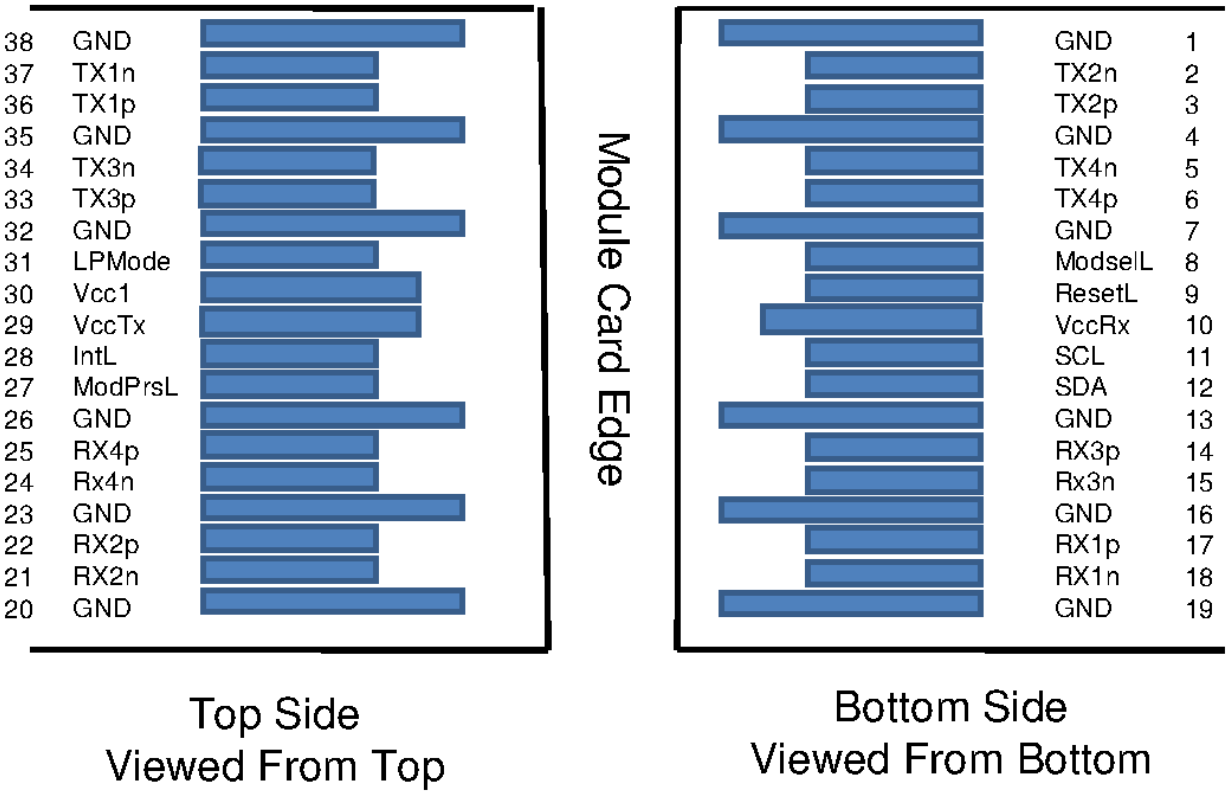

Fig 5. MODULE PAD LAYOUT

4. Electrical Pin Descriptions

Table 3. Pin Assignment

Pin	Logic	Symbol	Description	Plug Sequence
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3
7		GND	Ground	1
8	LVTTL-I	ModSelL	Module Select	3
9	LVTTL-I	ResetL	Module Reset	3
10		Vcc Rx	+3.3V Power Supply Receiver	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3
12	LVCMOS-I/O	SDA	2-wire serial interface data	3
13		GND	Ground	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3
15	CML-O	Rx3n	Receiver Inverted Data Output	3
16		GND	Ground	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3
18	CML-O	Rx1n	Receiver Inverted Data Output	3
19		GND	Ground	1
20		GND	Ground	1

21	CML-O	Rx2n	Receiver Inverted Data Output	3
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3
23		GND	Ground	1
24	CML-O	Rx4n	Receiver Non-Inverted Data Output	3
25	CML-O	Rx4p	Receiver Inverted Data Output	3
26		GND	Ground	1
27	LVTTL-O	ModPrsL	Module Present	3
28	LVTTL-O	IntL	Interrupt	3
29		Vcc Tx	+3.3V Power supply transmitter	2
30		Vcc1	+3.3V Power supply	2
31	LVTTL-I	LPMode	Low Power Mode	3
32		GND	Ground	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3
34	CML-I	Tx3n	Transmitter Inverted Data Input	3
35		GND	Ground	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3
37	CML-I	Tx1n	Transmitter Inverted Data Input	3
38		GND	Ground	1

5. Dimensions

Dimensions are in millimeters.

Tolerances are ±0.2mm, unless otherwise specified.

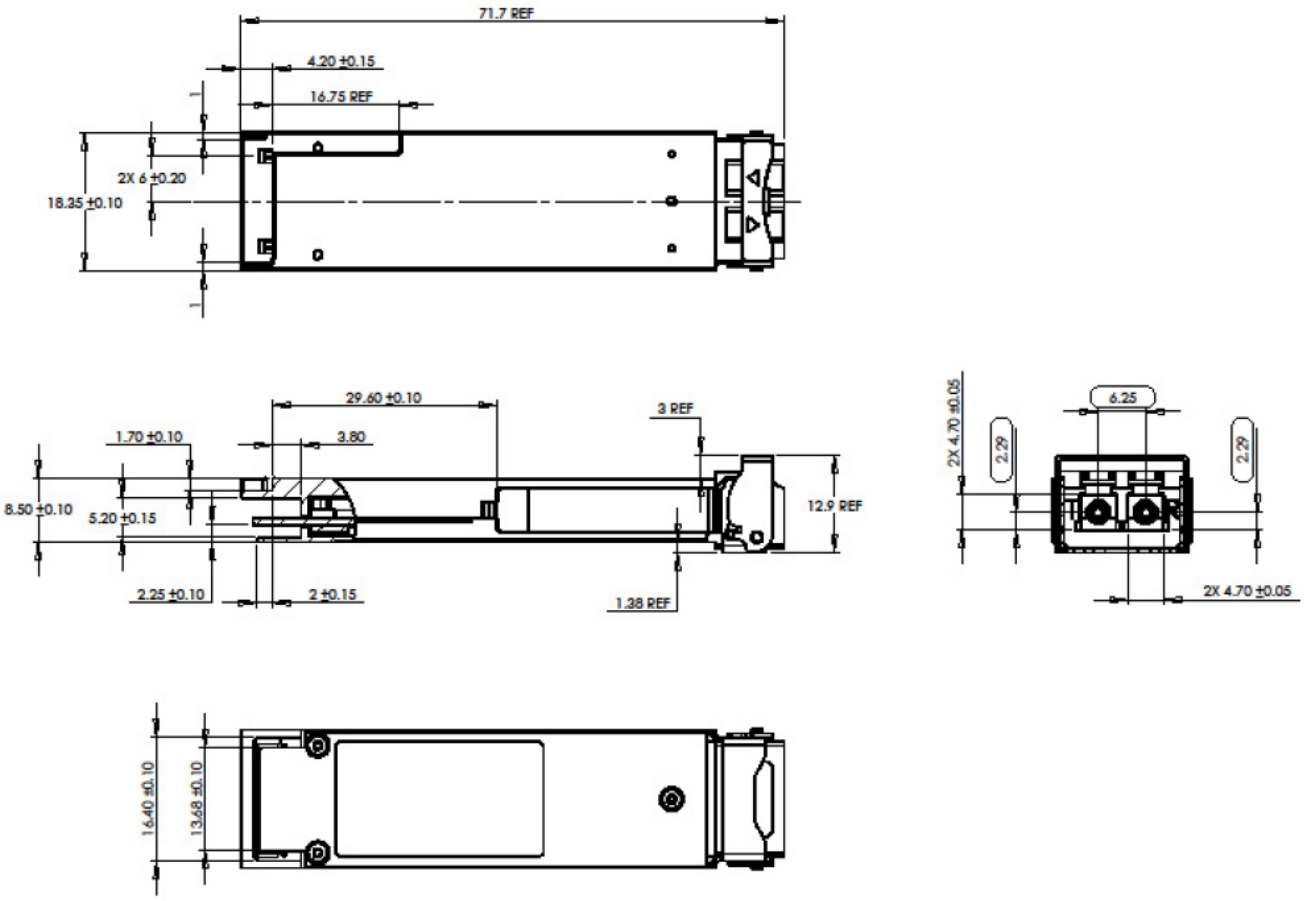

Fig 6. QSFP 28 Dimensions

6. Soft Control and Status Timing

Table 4. Soft Control &Status Timing Requirements

Parameter	Symbol	Max	Unit	Conditions
Initialization time	t_init	2000	ms	Time from power on, hot plug or rising edge of reset until the module is fully functional.
Reset Init Assert Time	t_rest_init	2	us	A Reset is generated by a low level longer than t_reset_init present on the ResetL input.
Serial Bus Hardware Ready Time	t_serial	2000	ms	Time from power on until the module responds to data transmission over the two-wire serial bus.
Monitor Data Ready Time	t_data	2000	ms	Time from power on to DataNotReady, byte 2 bit 0, deasserted and IntL output asserted.
Reset Assert Time	t_reset	2000	ms	Time from a rising edge on the ResetL input until the module is fully functional.
LPMode Assert Time	ton_LPMode	100	us	Time from assertion of LPMode (Vin:LPMode = Vih) until module power consumption reaches Power Level 1.
LPMode Deassert Time	toff_LPMode	300	ms	Time from deassertion of LPMode (Vin:LPMode = Vil) until module is fully functional.
IntL Assert Time	ton_IntL	200	ms	Time from occurrence of condition triggering IntL until Vout:IntL=Vol.
IntL Deassert Time	toff_IntL	500	us	Time from clear on read operation of associated flag until Vout:IntL=Voh. This includes deassert times for Rx LOS, Tx Fault and other flag bits.
Rx LOS Assert	ton_LOS	100	ms	Time from Rx LOS state to Rx LOS bit set (value = 1b) and IntL asserted.
Tx Fault Assert	tonTx_fault	200	ms	Time from Tx Fault state to Tx Fault bit set (value = 1b) and IntL asserted.
Flag Assert	ton_flag	200	ms	Time from condition triggering flag to associated flag bit set (value = 1b) and IntL asserted.
Mask Assert Time	ton_mask	100	ms	Time from mask bit set (value = 1b) until associated IntL assertion is inhibited.
Mask Deassert Time	toff_mask	100	ms	Time from mask bit cleared (value = 0b) until associated IntL operation resumes.
Application or Rate Select Change Time	T_ratesel	100	ms	Time from change of state of Application or Rate Select bit until transmitter or receiver bandwidth is in conformance with appropriate specification.

Power_override or Power_set Assert Time	ton_Pdown	100	ms	Time from P_Down bit set (value = 1b) until module power consumption reaches Power Level 1.
Power_override or Power_set Deassert Time	toff_Pdown	300	ms	Time from P_Down bit cleared (value = 0b) until module is fully functional.

7. Two-wire interface Protocol and Management Interface

2-Wire Serial Address 1010000x	
Lower Page 00h	
0	Identifier
1 - 2	Status
3 - 21	Interrupt Flags
22 - 33	Module Monitors
34 - 81	Channel Monitors
82 - 85	Reserved
86 - 98	Control
99	Reserved
100 - 106	Free Side Device and Channel Mask
107	Reserved
108 - 112	Free Side Device Properties
113 - 118	Reserved
119 - 122	Password Change Entry Area (Optional)
123 - 126	Password Entry Area(Optional)
127	Page Select Byte

Upper Page 00h	
128	Identifier
129 - 191	Base ID Fields
192 - 223	Extended ID
224 - 255	Vendor Specific ID

Optional	
Page 01h	
128	CC_APPS
129	AST Table Length (TL)
130 - 131	Application Code Entry 0
132 - 133	Application Code Entry 1
134 - 253	Other entries
254 - 255	Application Code Entry TL

Optional	
Page 02h	
128 - 255	User EEPROM Data

Optional	
Page 03h(Cable Assemblies)	
128 - 175	Free Side Device Thresholds
176 - 223	Channel Threshold
224 - 225	Reserved
226 - 227	Vendor
238 - 241	Channel Controls
242 - 253	Channel Monitor Masks
254 - 255	Reserved

Fig 7. Memory map

8. Specification

8.1. Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Unit
Storage Temperature	T_{ST}	-40		+85	℃
Power Supply Voltage	V_{CC}	0		3.6	V
Operating Humidity	H_{OP}			85	% RH

8.2. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Operating Case Temperature	T_c	0		70	℃
Supply Voltage	V_{CC}	3.135	3.3	3.465	V
Power Consumption	P_W			TBD	W

8.3. Transmitter Characteristics

Parameter		Symbol	Min	Typ	Max	Unit
Signaling rate, each lane(range)		B	25.78125 ± 100 ppm			GBd
			27.9525 ± 20 ppm			
Lane Wavelength (range)	Lane 0	λ_c	1294.53	1295.56	1296.59	nm
	Lane 1		1299.02	1300.05	1301.09	
	Lane 2		1303.54	1304.58	1305.63	
	Lane 3		1308.09	1309.14	1310.19	
Side-mode suppression ratio(SMSR)			30			dB
Total average launch power					10.5	dBm
Average launch power, each lane			-4.3		4.5	dBm
Transmitter and dispersion penalty, each lane					2.2	dB
Average launch power of OFF transmitter, each lane					-30	dBm
Extinction ratio			4			dB
RIN OMA					-130	dB/Hz
Optical return loss tolerance					20	dB
Transmitter reflectance					-12	dB

8.4. Receiver Characteristics

Parameter		Symbol	Min	Typ	Max	Unit
Signaling rate, each lane(range)		B	25.78125 ± 100 ppm			GBd
			27.9525 ± 20 ppm			
Lane Wavelength (range)	Lane 0	λ_c	1294.53	1295.56	1296.59	nm
	Lane 1		1299.02	1300.05	1301.09	
	Lane 2		1303.54	1304.58	1305.63	
	Lane 3		1308.09	1309.14	1310.19	
Damage threshold			5.5			dBm
Average receive power, each lane			-10.6		4.5	dBm
Receiver reflectance					-26	dB
Receiver sensitivity, each lane					-8.6	dBm

9. ESD(Electrostatic Discharge)

The module speed signal contacts shall withstand 1000 V electrostatic discharge based on Human Body Model per JEDEC JESD22-A114-B.

10, Laser Safety

The transceivers use a semiconductor laser that is classified as Class 1 laser products per the laser safety requirements of FDA/CDRH, 21 CFR1040.10 and 1040.11. These products have also been tested and certified as Class 1 laser products per IEC60825-1:2007 and IEC60825-1:2001 International standards.

11. Ordering Information

For more information on this or other products and their availability, please contact e-mail at sales@intecec.com.

①	②	-	③	④	⑤	⑥	-	⑦	⑧	⑨

No.	ITEM	Code	Description
①	Company	I	INTEC E&C
②	Form Factor	Q2	QSFP 28
③	Data-rate	CE	100Gbps
④	Distance	LR	10Km
⑤	Wavelength	LW	LAN-WDM
⑥	Optical interface	B	LC-UPC receptacle
⑦	Temperature range	S	0℃ ~ 70℃(Case temp.)
⑧	Lane	04	4 Channel
⑨	customer	I	-

12. Revision History

1. Version 0.1(dated 2015-04-17)
   : Initial Release

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